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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
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| 09/940,885 | 08/29/2001 | Masahiro Kawasaki | 500.45062X00 | 5638 |

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| EXAMINER | |
|---|---|
| ERDEM, FAZLI | |

| ART UNIT | PAPER NUMBER |
|---|---|
| 2826 | |

DATE MAILED: 02/20/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 09/940,885 | KAWASAKI ET AL. | |
| | Examiner | Art Unit | |
| | Fazli Erdem | 2826 | |

*-- The MAILING DATE of this communication appears on the cov r sh t with the correspond nce address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *Amendment filed on 11/18/2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-25* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *9 and 14-25* is/are allowed.

6)☒ Claim(s) *1,6-8 and 10-13* is/are rejected.

7)☒ Claim(s) *2-5* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *12/15/2003*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

## DETAILED ACTION

### *Allowable Subject Matter*

1. Claims 9 and 14-25 allowed

2. Claim 2-5 objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

### *Claim Rejections - 35 USC § 103*

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1 and 6-8 rejected under 35 U.S.C. 103(a) as being unpatentable over Fukunaga (6,271,101) in view of Yamazaki et al. (6,335,231) further in view of Yamazaki et al. (6,362,027).

Regarding Claims 1-8, Fukunaga discloses a process for production of SOI substrate and process for production of semiconductor device where a process for producing an adhered SOI substrate without causing cracking and peeling of a single-crystal silicon thin film. The process consists of selectively forming a porous silicon layer in a single-crystal semiconductor substrate, adding hydrogen into the single-crystal semiconductor substrate to form a hydrogen-added layer, adhering the single crystal semiconductor substrate to a supporting substrate, separating the single-crystal semiconductor substrate at the hydrogen-added layer by thermal annealing,

performing thermal annealing again to stabilize the adhering interface, and selectively removing the porous silicon layer to give single-crystal silicon layer divided into islands. Fukunaga fails to disclose the required laminate/porous structure and the passivation structure. However, Yamazaki et al. (231) disclose a method of fabricating a high reliable SOI substrate where the required laminate/porous structure is disclosed. Furthermore, Yamazaki et al. (027) disclose a semiconductor device, active matrix substrate, method of manufacturing the semiconductor device and method of manufacturing the active matrix substrate where the required passivation structure is disclosed.

It would have been obvious to one of having ordinary skill in the art at the time the invention was made to include the required laminate/porous structure and the passivation structure in Fukunaga as taught by Yamazaki et al. and Yamazaki et al. respectively in order to have a semiconductor device with better performance.

4. Claims 10 and 11 rejected under 35 U.S.C. 103(a) as being unpatentable over Zhang (6,140,164) in view of Yamazaki et al. (6,335,231) further in view of Yamazaki et al. (6,362,027) further in view of Sakaguchi et al. (6,054,363)

Regarding Claims 10 and 11, Zhang discloses a method of manufacturing a semiconductor device where a resist mask used for forming a region of aluminum is made small by ashing to form a new mask. Anodic oxidation is carried out with an anode of the region of aluminum to form porous anodic oxidation films. This way, mask can control the directions of openings of the porous anodic oxidation films. If the impurity ions are implanted using the porous anodic oxidation films as masks, the amount of impurity ions implanted into an active

layer can be adjusted. Zhang fails to disclose the required fails to disclose the required laminate/porous structure, passivation structure, and the ion irridating structure. However, Yamazaki et al. (231) disclose a method of fabricating a high reliable SOI substrate where the required laminate/porous structure is disclosed. Furthermore, Yamazaki et al. (027) disclose a semiconductor device, active matrix substrate, method of manufacturing the semiconductor device and method of manufacturing the active matrix substrate where the required passivation structure is disclosed. Finally, Sakaguchi et al. disclose a method of manufacturing semiconductor article where the required ion irradiating structure is disclosed.

It would have been obvious to one of having ordinary skill in the art at the time the invention was made to include the required laminate/porous structure, passivation structure, and the ion irradiating structure in Zhang as taught by Yamazaki et al., Yamazaki et al., and Sakaguchi et al. respectively in order to make a semiconductor device with better performance.

5. Claims 12 and 13 rejected under 35 U.S.C. 103(a) as being unpatentable over Konuma et al. (5,747,355) in view of Yamazaki et al. (6,335,231) further in view of Yamazaki et al. (6,362,027) further in view of Sakaguchi et al. (6,054,363).

Regarding Claims 12 and 13, Konuma et al. disclose a method for producing a transistor using anodic oxidation where a method for producing a thin-film transistor in which the gate electrode is offset from the source and drain without detriment to the characteristics of the device or to manufacturing yield, and a structure for such a TFT are disclosed. Konuma et al. fail to disclose the required fails to disclose the required laminate/porous structure, passivation structure, and the ion irridating structure. However, Yamazaki et al. (231) disclose a method of

fabricating a high reliable SOI substrate where the required laminate/porous structure is disclosed. Furthermore, Yamazaki et al. (027) disclose a semiconductor device, active matrix substrate, method of manufacturing the semiconductor device and method of manufacturing the active matrix substrate where the required passivation structure is disclosed. Finally, Sakaguchi et al. disclose a method of manufacturing semiconductor article where the required ion irradiating structure is disclosed.

It would have been obvious to one of having ordinary skill in the art at the time the invention was made to include the required laminate/porous structure, passivation structure, and the ion irradiating structure in Konuma et al. as taught by Yamazaki et al., Yamazaki et al. and Sakaguchi et al. respectively in order to make a semiconductor device with better performance.

***Conclusion***

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Fazli Erdem whose telephone number is (703) 305-3868. The examiner can normally be reached on M - F 8:00 - 5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan Flynn can be reached on (703) 308-6601. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 308-7722 for regular communications and (703) 308-7724 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

Starting February 4, 2004, Examiner Fazli Erdem's phone number will be changed to (571) 272-1914 and his SPE Nathan Flynn's phone number will be changed to (571) 272-1915

FE
February 8, 2004

NATHAN J. FLYNN
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800